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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,181	01/12/2001	Naoki Matsuoka	FUJY 17.298	9982

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EXAMINER	
CANGIALOSI, SALVATORE A	
ART UNIT	**PAPER NUMBER**
2661	6

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,181	MATSUOKA ET AL.	
	Examiner	Art Unit	
	Salvatore Cangialosi	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,10-13 and 16-18* is/are rejected.

7)☒ Claim(s) *3-9,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3,5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

2. Claims 1, 2, 10-13, 16-18 are rejected under 35 U.S.C. § 103 as being unpatentable over Lund et al in view of either Kawaei et al or Mekkitikul(Both cited by applicant).

Regarding claim 1, Lund et al (See Fig. 1 and claim 1) disclose a packet switch means with a plurality of input buffers, buffer control means and a scheduling means substantially as claimed. It is noted that the packets are assembled into a frame of fixed length packets. The differences between the above and the claimed invention are the specific parallel or pipeline processing by the scheduling means. Note that buffer control means must also send back control messages to the input buffers which are the functional equivalent of status management that both manages(controls) and notifies the input

buffers(sends the control signal). Either Kawaei et al(See Fig. 1 and 5 and paragraph 3.2) or Mekkitikul (paragraph 4.1.1 PIPELINE TECHNIQUE) show typical parallel or pipeline scheduling. It would have been obvious to the person having ordinary skill in this art to provide a similar arrangement Lund et al because it is well known that parallel processing is faster than serial processing in the prior art and would increase switch and network response time. Regarding the scheduling limitations of claim 2, either Kawaei et al(See Fig. 1 and 5 and paragraph 3.2) or Mekkitikul (paragraph 4.1.1 PIPELINE TECHNIQUE) show typical parallel or pipeline scheduling which are the functional equivalents of the claim. Regarding claim 10, Lund et al (See Fig. 1 and claim 1) disclose a packet switch means with a plurality of input buffers, buffer control means and a scheduling means substantially as claimed. It is noted that the packets are assembled into a frame of fixed length packets. The differences between the above and the claimed invention are the specific processing by the scheduling means of variable length frames. Note that buffer control means must also send back control messages to the input buffers which are the functional equivalent of status management that both manages (controls) and notifies the input buffers(sends the control signal). Either Kawaei et al(See Fig. 1 and 5 and paragraph 3.2) or Mekkitikul (paragraph 4.1.1 PIPELINE TECHNIQUE) show typical parallel or pipeline scheduling which allow for variable frame processing. It would have been obvious to the

person having ordinary skill in this art to provide a similar arrangement Lund et al because it is well known that parallel processing is faster than serial processing in the prior art and would increase switch and network response time for variable frame processing. Regarding claim 11, Lund et al (See Fig. 1 and claim 1) disclose a packet switch method with a plurality of input buffers, buffer control means and a scheduling means substantially as claimed. It is noted that the packets are assembled into a frame of fixed length packets. The differences between the above and the claimed invention are the specific parallel or pipeline processing by the scheduling means. Note that buffer control means must also send back control messages to the input buffers which are the functional equivalent of status management that both manages(controls) and notifies the input buffers(sends the control signal). Either Kawaei et al(See Fig. 1 and 5 and paragraph 3.2) or Mekkitikul (paragraph 4.1.1 PIPELINE TECHNIQUE) show typical parallel or pipeline scheduling. It would have been obvious to the person having ordinary skill in this art to provide a similar arrangement Lund et al because it is well known that parallel processing is faster than serial processing in the prior art and would increase switch and network response time. Regarding the scheduling limitations of claim 12, Lund et al (See Fig. 1 and claim 1) show buffer control means which must also send back control messages to the input buffers which are the functional equivalent of status management that both

manages(controls) and notifies the input buffers(sends the control signal). Regarding the scheduling limitations of claim 13, either Kawaei et al(See Fig. 1 and 5 and paragraph 3.2) or Mekkitikul (paragraph 4.1.1 PIPELINE TECHNIQUE) show typical parallel or pipeline scheduling which are the functional equivalents of the claim. Regarding claim 16, Lund et al (See Fig. 1 and claim 1) disclose a packet switch means with a plurality of input buffers, buffer control means and a scheduling means substantially as claimed. It is noted that the packets are assembled into a frame of fixed length packets. The differences between the above and the claimed invention are the specific processing by the scheduling means. Note that buffer control means must also send back control messages to the input buffers which are the functional equivalent of status management that both manages(controls) and notifies the input buffers(sends the control signal). Either Kawaei et al(See Fig. 1 and 5 and paragraph 3.2) or Mekkitikul (paragraph 4.1.1 PIPELINE TECHNIQUE) show typical parallel or pipeline scheduling which would assemble a frame. It would have been obvious to the person having ordinary skill in this art to provide a similar arrangement Lund et al because it is well known that parallel processing is faster than serial processing in the prior art and would increase switch and network response time in frame assembly. Regarding claim 17, Lund et al (See Fig. 1 and claim 1) disclose a packet switch means with a plurality of input buffers, buffer control means and

a scheduling means substantially as claimed. It is noted that the packets are assembled into a frame of fixed length packets. The differences between the above and the claimed invention are the specific processing by the scheduling means of variable length frames. Note that buffer control means must also send back control messages to the input buffers which are the functional equivalent of status management that both manages (controls) and notifies the input buffers(sends the control signal). Either Kawaei et al(See Fig. 1 and 5 and paragraph 3.2) or Mekkitikul (paragraph 4.1.1 PIPELINE TECHNIQUE) show typical parallel or pipeline scheduling which allow for variable frame processing. It would have been obvious to the person having ordinary skill in this art to provide a similar arrangement Lund et al because it is well known that parallel processing is faster than serial processing in the prior art and would increase switch and network response time for variable frame processing. Regarding claim 18, Lund et al (See Fig. 1 and claim 1) disclose a packet switch method with a plurality of input buffers, buffer control means and a scheduling means substantially as claimed. It is noted that the packets are assembled into a frame of fixed length packets. The differences between the above and the claimed invention are the specific parallel or pipeline processing by the scheduling means. Note that buffer control means must also send back control messages to the input buffers which are the functional equivalent of status management that both manages(controls) and notifies the

input buffers(sends the control signal). Either Kawaei et al(See Fig. 1 and 5 and paragraph 3.2) or Mekkitikul (paragraph 4.1.1 PIPELINE TECHNIQUE) show typical parallel or pipeline scheduling. It would have been obvious to the person having ordinary skill in this art to provide a similar arrangement Lund et al because it is well known that parallel processing is faster than serial processing in the prior art and would increase switch and network response time to form a frame.

Claims 3-9 and 14-15 are objected to as being dependent on rejected claims.

Any inquiry concerning this communication should be directed to Salvatore Cangialosi at telephone number (703) 305-1837. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Olms, can be reached at (703) 305-4703.

Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

or faxed to (703)872-9306

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, Virginia, Sixth Floor(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

SALVATORE CANGIALOSI
PRIMARY EXAMINER
ART UNIT 222